REMARKS

Claims 1-14, 23-26, and 31-44 will be pending upon entry of the present amendment. Claims 1 and 4 are being amended. Claims 33-44 are new.

Claims 1-14, 23-26, and 31-32 were rejected under 35 U.S.C. § 103 as being unpatentable over United States Patent No. 6,127,723 to Aiello et al. ("Aiello") in view of U.S. Patent No. 6,207,481 to Yi et al. ("Yi").

The cited prior art does not teach or suggest the invention recited in the pending claims. For example, claim 1 recites an integrated device that includes a quenching element having a Zener diode made in polysilicon and formed on a second surface of a semiconductor chip and comprising a polysilicon layer having at least one zone of the first conductivity type and at least one zone of a second conductivity type in order to form at least one P-N junction. Aiello and Yi do not teach or suggest such a quenching element connected as recited in claim 1, for at least two reasons.

First, there is no motivation to combine Aiello with Yi to produce the claimed invention. Aiello shows a diode D1 formed in a monocrystalline epitaxial layer 218 while Yi shows a thin film transistor formed in a polysilicon layer 218. Nothing in Aiello, Yi, or the general knowledge of the prior art provides a reason to replace the monocrystalline diode D1 with the thin film transistor of Yi. The Examiner mistakenly asserts that Yi teaches that using polysilicon results in a uniform crystal size and better transistor performance. A primary basis of the entire semiconductor industry is that a transistor integrated in a single crystal of silicon provides better transistor performance than a transistor formed in a polysilicon layer. If that were not true, then semiconductor companies would not need to spend the time and expense producing monocrystalline silicon chips. Further, by definition, a single crystal of silicon has a perfectly uniform crystal size because there is only one crystal size. Rather than comparing polysilicon to monocrystalline silicon, as in Aiello, Yi simply reports that the method of producing a polysilicon layer in Yi is better than prior art methods of producing polysilicon layers. As such, Yi's teaching does not provide a suggestion or motivation for replacing the monocrystalline diode D1 with the thin film transistor of Yi.

Second, even if one were motivated to employ the thin film transistor of Yi on the structure of Aiello, one still would not create the claimed invention. Claim 1 recites that the quenching element, which includes a polysilicon PN junction, is coupled with the base region of the first transistor and with the not drivable terminal of the second transistor. Neither Aiello nor Yi suggest connecting a polysilicon PN junction to a base region or not drivable terminal of integrated transistors. In particular, Yi does not connect the thin film transistor of layer 118 to any regions or terminals of any transistors in the substrate 111. Thus, a hypothetical combination of Yi with Aiello would at most merely position the thin film transistor of Yi in a polysilicon layer above the structure of Aiello, without connecting the thin film transistor as a quenching element between the base terminal of a first transistor and a not drivable terminal of a second transistor.

For the foregoing reasons, claim 1 is nonobvious in view of the cited prior art.

Claims 2-14, 31, and 33 depend on claim 1, and thus, are likewise nonobvious in view of the cited prior art. In addition, claims 2-4, 31, and 33 recite many other features not taught or suggested by the cited prior art. For example, new claim 33 recites that the emitter region of the first transistor extends as a comb having elongated portions inside the base region and the polysilicon region includes a plurality of zener diodes distributed along a perimeter of the elongated portions. Neither Aiello nor Yi teaches or suggests such an arrangement.

Although the language of claims 23-26, 32, and 34-44 differs from that of claims 1-14, 31, and 33, the allowability of claims 23-26, 32, and 34-44 will be apparent in view of the above discussion.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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